MAX17701

4.5V to 60V, Synchronous Step-Down Supercapacitor Charger Controller

General Description

The Himalaya series of voltage regulator ICs, power modules, and chargers enable cooler, smaller, and simpler power supply solutions. The MAX17701 is a high efficiency, high voltage, Himalaya synchronous, step-down, supercapacitor charger controller designed to operate over an input-voltage range of a 4.5V to 60V. The MAX17701 operates over a -40°C to +125°C industrial temperature range and charges a supercapacitor with a ±4% accurate constant current. After the supercapacitor is charged, the device regulates the no-load output voltage with ±1% accuracy. The output voltage is programmable from 1.25V up to (V_{DCIN} - 4V).

The MAX17701 supercapacitor charger controller is designed to provide a holistic application solution requiring backup energy storage with a precise charging capability. The device uses an external nMOSFET to provide input supply-side short-circuit protection; thus, preventing supercapacitor discharge.

The MAX17701 provides a safety timer (TMR) feature to set the maximum allowed constant current (CC) mode charging time. The device features an uncommitted comparator, which can be used to detect an output overvoltage event (OVI) and prevent the supercapacitor from overcharging. The MAX17701 is available in a 24-pin 4mm x 4mm TQFN package with an exposed pad.

Applications

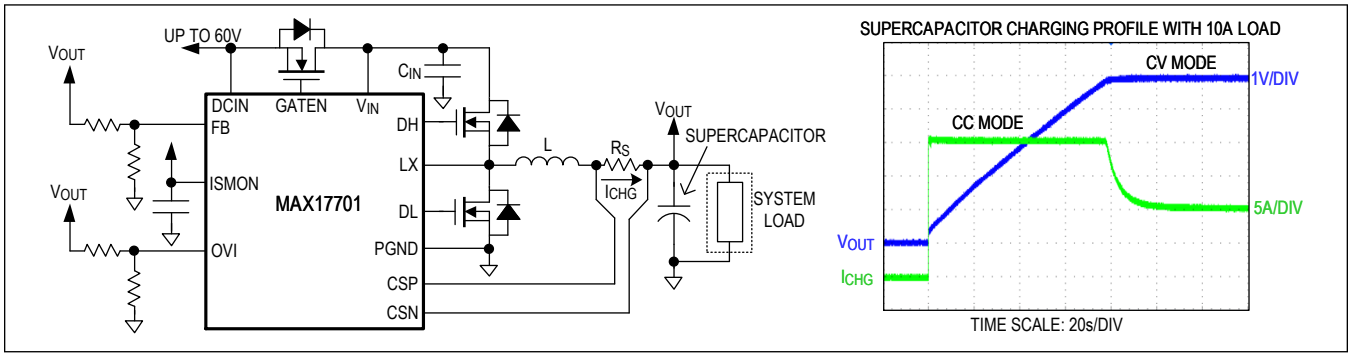
- Peak Power Delivery and Energy Storage
- Backup Power for Industrial Safety
- Ride-Through Last-Gasp Supplies
- Portable Medical Equipment
- Building and Home Automation Backup Power

Benefits and Features

- Optimized Feature Set for Supercapacitor Charging
  - ±4% Charging Current Regulation Accuracy
  - ±6% Charging Current Monitor Accuracy (ISMON)
  - ±1% Voltage Regulation Accuracy
  - Programmable CC Mode Charging Current (ILIM)
  - Wide 4.5V to 60V Input-Voltage Range
  - Adjustable Output-Voltage Range from 1.25V Up To (V_{DCIN} - 4V)
  - 125kHz to 2.2MHz Adjustable Frequency with External Clock Synchronization (RT/SYNC)
- Reliable Operation in Adverse Environmental Conditions
  - Input Short-Circuit Protection (GATEN)
  - Safety Timer Feature (TMR)
  - Output Overvoltage Protection (OVI)
  - Cycle-by-Cycle Overcurrent Limit
  - Programmable EN/UVLO Threshold
  - Fault Monitoring Open-Drain Output ($\overline{FLG}$)
  - Overtemperature Protection
  - Wide -40°C to +125°C Ambient Operating Temperature Range/ -40°C to +150°C Junction Temperature Range

***Ordering Information* appears at end of data sheet.**

Simplified Application Circuit



maxim integrated™

Absolute Maximum Ratings

V_{IN} to SGND/EP ..... -0.3V to +65V
DCIN to SGND/EP ..... -0.3V to min(+65V, V_{IN} + 0.6V)
GATEN to SGND/EP .... max(-0.3V, DCIN - 0.3V) to (DCIN + 6V)
GATEN to DCIN ..... -0.3V to +6V
V_{CC} to SGND/EP ..... -0.3V to min(+6V, V_{IN} + 0.3V)
CSN, CSP to SGND/EP ..... -0.3V to (V_{IN} + 0.6V)
CSP to CSN ..... -0.3V to +0.3V
V_{REF}, TMR, ILIM to SGND/EP ..... -0.3V to (V_{CC} + 0.3V)
COMP, ISMON, RT/SYNC to SGND/EP .... -0.3V to (V_{CC} + 0.3V)
$\overline{OVI}$, FB to SGND/EP ..... -0.3V to +6V
$\overline{FLG}$, EN/UVLO to SGND/EP ..... -0.3V to +6V
LX to PGND ..... -0.3V to +65V
BST to LX ..... -0.3V to +6V
BST to PGND ..... -0.3V to +70V
DL to PGND ..... -0.3V to (V_{CC}+ 0.3V)
DH to LX ..... -0.3V to (BST + 0.3V)
EXTVCC to SGND/EP ..... -0.3V to +26V
PGND, IC1, IC2 to SGND/EP ..... -0.3V to +0.3V
Continuous Power Dissipation (TA = +70°C) (TQFN (derate 27.85mW/°C above +70°C)) 2222mW
Operating Temperature Range (Note 1) .....-40°C to +125°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s).....+300°C
Soldering Temperature (reflow) .....+260°C

Note 1: Junction temperature greater than +125°C degrades operating lifetimes.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

24 PIN TQFN

Package Code	T2444+5C
Outline Number	21-100405
Land Pattern Number	90-100139
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	36°C/W
Junction to Case (θ_{JC})	3°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{IN} = V_{DCIN} = 24V, C_{VIN} = 4.7µF, C_{DCIN} = 100nF, C_{VCC} = 4.7µF, C_{VREF} = 100nF, C_{BST} = 470nF, V_{EXTVCC} = $V_{SGND/EP}$ = V_{PGND} = V_{FB} = $V_{\overline{OVI}}$ = V_{IC2} = 0V, $V_{EN/UVLO}$ = V_{LX} = V_{TMR} = V_{ILIM} = V_{CSN} = V_{CSP} = 2.5V, V_{BST} to V_{LX} = 5V, RT/SYNC = DH = DL = GATEN = COMP = $\overline{FLG}$ = ISMON = IC1 = Unconnected, T_A= -40°C to +125°C, unless otherwise noted. Typical values are at T_A= +25°C. All voltages are referenced to SGND/EP, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
DCIN Voltage Range		DCIN connected to V_{IN}, External nMOSFET not used	4.5		60	V
		External nMOSFET used	5.5		60	
V_{IN} Voltage Range			4.5		60	V
Input Quiescent Current	I_{QNS}	(V_{IN} - V_{CSN}) > 2.1V, V_{FB} = 1.5V	1.4	2.1	2.8	mA
Input Switching Current	I_{QS}		1.7	2.5	3.5	mA
Shutdown Supply Current	I_{IN-SH}	$V_{EN/UVLO}$ = 0V (Shutdown mode)		7	18	µA

Electrical Characteristics (continued)

(V_{IN} = V_{DCIN} = 24V, C_{VIN} = 4.7µF, C_{DCIN} = 100nF, C_{VCC} = 4.7µF, C_{VREF} = 100nF, C_{BST} = 470nF, V_{EXTVCC} = $V_{SGND/EP}$ = V_{PGND} = V_{FB} = V_{OVI} = V_{IC2} = 0V, $V_{EN/UVLO}$ = V_{LX} = V_{TMR} = V_{ILIM} = V_{CSN} = V_{CSP} = 2.5V, V_{BST} to V_{LX} = 5V, RT/SYNC = DH = DL = GATEN = COMP = $\overline{FLG}$ = ISMON = IC1 = Unconnected, T_A= -40°C to +125°C, unless otherwise noted. Typical values are at T_A= +25°C. All voltages are referenced to SGND/EP, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ENABLE/UVLO (EN/UVLO)						
EN/UVLO Rising Threshold	$V_{EN\_TH\_R}$	$V_{EN/UVLO}$ rising	1.22	1.25	1.27	V
EN/UVLO Falling Threshold	$V_{EN\_TH\_F}$		1.07	1.09	1.11	V
EN/UVLO Bias Current	$I_{EN-BIAS}$	$V_{EN/UVLO}$ = 0.5V	1.4	3.0	6.5	µA
EN/UVLO True Shutdown Threshold	V_{ENT}	$V_{EN/UVLO}$ rising	0.4	0.7	1.1	V
		Hysteresis		60		mV
V_{CC} REGULATORS (INT-LDO AND EXT-LDO)						
V_{CC} Output Voltage	V_{CC}	6V < V_{IN} < 60V, I_{VCC} = 1mA (V_{CC} supplied from INT-LDO)	5.00	5.15	5.30	V
		V_{IN} = 24V, I_{VCC} = 0mA to 75mA, (V_{CC} supplied from INT-LDO)	4.95	5.10	5.25	
		6V < V_{EXTVCC} < 24V, I_{VCC} = 1mA (V_{CC} supplied from EXT-LDO)	5.00	5.15	5.30	
		V_{EXTVCC} = 12V, I_{VCC} = 0mA to 75 mA, (V_{CC} supplied from EXT-LDO)	4.95	5.10	5.25	
V_{CC} Output Current Limit	I_{VCC_LIMIT}	V_{IN} = 8.5V, V_{CC} = 4V (V_{CC} supplied from INT-LDO)	80	110	135	mA
		V_{EXTVCC} = 8.5V, V_{CC} = 4V (V_{CC} supplied from EXT-LDO)	80	110	135	
V_{CC} Dropout Voltage	V_{CC-DO}	V_{IN} = 4.5V, I_{VCC} = 75mA (V_{CC} supplied from IN-LDO)		370	750	mV
		V_{EXTVCC} = 4.9V, I_{VCC} = 75mA (V_{CC} supplied from EXT-LDO)		185	350	
V_{CC} Undervoltage Threshold	V_{CC-UVR}	V_{CC} rising	4.14	4.20	4.26	V
	V_{CC-UVF}	V_{CC} falling	3.74	3.80	3.86	
EXTVCC Voltage Range			4.8		24.0	V
EXTVCC Switchover Voltage		V_{EXTVCC} rising	4.63	4.70	4.77	V
		Hysteresis		0.24		
OSCILLATOR (RT/SYNC)						
Switching Frequency	f_{SW}	$R_{RT/SYNC}$ = 350 kΩ	118.75	125.00	131.25	kHz
		$R_{RT/SYNC}$ = Unconnected	332.5	350.0	367.5	
		$R_{RT/SYNC}$ = 110kΩ	380	400	420	
		$R_{RT/SYNC}$ = 19kΩ	2090	2200	2310	
Synchronization Frequency Range	f_{SYNC}		0.9 x f_{SW}		1.1 x f_{SW}	kHz
External Clock Amplitude		$C_{COUPLING}$ = 10pF	3			V

Electrical Characteristics (continued)

(V_{IN} = V_{DCIN} = 24V, C_{VIN} = 4.7µF, C_{DCIN} = 100nF, C_{VCC} = 4.7µF, C_{VREF} = 100nF, C_{BST} = 470nF, V_{EXTVCC} = $V_{SGND/EP}$ = V_{PGND} = V_{FB} = V_{OVI} = V_{IC2} = 0V, $V_{EN/UVLO}$ = V_{LX} = V_{TMR} = V_{ILIM} = V_{CSN} = V_{CSP} = 2.5V, V_{BST} to V_{LX} = 5V, RT/SYNC = DH = DL = GATEN = COMP = $\overline{FLG}$ = ISMON = IC1 = Unconnected, T_A= -40°C to +125°C, unless otherwise noted. Typical values are at T_A= +25°C. All voltages are referenced to SGND/EP, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYNC High Pulse-Width			100			ns
SYNC Low Pulse-Width			100			ns
SYNC Input-Leakage Current	I_{SYNC_LKG}	$V_{RT/SYNC}$ = 2.5V, T_A= +25ºC	-100		+100	nA
GATE DRIVER						
DH to BST On-Resistance		Source 100mA	0.8	1.2	2.1	Ω
DH to LX On-Resistance		Sink 100mA	0.3	0.6	1.0	Ω
DL to V_{CC} On-Resistance		Source 100mA	0.8	1.2	2.1	Ω
DL to PGND On-Resistance		Sink 100mA	0.3	0.6	1.0	Ω
DH Minimum Controlled On Time	$t_{MIN\_ON\_DH}$		60	80	100	ns
DL Minimum Guaranteed On Time	$t_{MIN\_ON\_DL}$		60	80	100	ns
Dead Time	t_{DT_HL}	DH falling to DL rising, C_{DH-LX} = 6nF, $C_{DL-PGND}$ = 6nF		30		ns
	t_{DT_LH}	DL falling to DH rising, C_{DH-LX} = 6nF, $C_{DL-PGND}$ = 6nF		30		
DH Transition Time	t_{HR}	DH rising, C_{DH-LX} = 6nF		25		ns
	t_{HF}	DH falling, C_{DH-LX} = 6nF		11		
DL Transition Time	t_{LR}	DL rising, $C_{DL-PGND}$ = 6nF		25		ns
	t_{LF}	DL falling, $C_{DL-PGND}$ = 6nF		11		
REFERENCE VOLTAGE (VREF)						
V_{REF} Output Voltage	V_{REF}	I_{VREF} = 0 to 1mA	2.465	2.500	2.535	V
Reference Current Limit	I_{REF_LIM}	V_{REF} = 2.45V	1.2	1.8	2.7	mA
CURRENT SENSE (CSP, CSN, ILIM)						
CSP, CSN Common Mode Voltage Range			0		(V_{IN} - 2)	V
CSP to CSN Input Operating Voltage	V_{DIFF_CS}	V_{DIFF_CS} = (V_{CSP} - V_{CSN})	-10		+100	mV
CSP to CSN Regulation Voltage Accuracy	V_{CSREG}	V_{ILIM} = 1.5V	48	50	52	mV
		V_{ILIM} = 0.75V	23	25	27	
		V_{ILIM} = 0.15V	3	5	7	
		V_{ILIM} = V_{REF}	48	50	52	
CSP Pin Current		CSP source	20	200	3700	nA

Electrical Characteristics (continued)

(V_{IN} = V_{DCIN} = 24V, C_{VIN} = 4.7µF, C_{DCIN} = 100nF, C_{VCC} = 4.7µF, C_{VREF} = 100nF, C_{BST} = 470nF, V_{EXTVCC} = $V_{SGND/EP}$ = V_{PGND} = V_{FB} = V_{OVI} = V_{IC2} = 0V, $V_{EN/UVLO}$ = V_{LX} = V_{TMR} = V_{ILIM} = V_{CSN} = V_{CSP} = 2.5V, V_{BST} to V_{LX} = 5V, RT/SYNC = DH = DL = GATEN = COMP = $\overline{FLG}$ = ISMON = IC1 = Unconnected, T_A= -40°C to +125°C, unless otherwise noted. Typical values are at T_A= +25°C. All voltages are referenced to SGND/EP, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CSN Pin Current		$V_{EN/UVLO}$ = 0V, CSN sink			1.3	2.3	µA
		Charger on, V_{ILIM} = 0.15V to 1.5V (see Note 3)	I_{CHG} > I_{CHGMAX}/10, CSN source	250	400	550	
			I_{CHG} < I_{CHGMAX}/10, CSN sink	470	700	1000	
Current Loop Error Amplifier Transconductance	g_{mi}	(V_{CSP} - V_{CSN}) = V_{CSNEG} ±25mV		275	480	685	µS
ILIM Input-Leakage Current		V_{ILIM} = 1.5V, T_A = +25ºC		-100		+100	nA
CSN Undervoltage-Lockout Threshold	V_{CMUVLO}	(V_{IN} - V_{CSN}), rising		1.97	2.04	2.10	V
		(V_{IN} - V_{CSN}), falling		1.88	1.95	2.02	
Overcurrent Threshold	V_{CSPEAK}	V_{CSPEAK} = (V_{CSP} - V_{CSN}), V_{ILIM} = 1.5V		70	75	80	mV
		Hysteresis			10		
Zero Cross Threshold	V_{ZX}	(V_{CSP} - V_{CSN}) falling		-3.7	-1.7	-0.2	mV
PWM Ramp Amplitude	V_{RAMP}	f_{SW} = 125kHz to 2.2MHz		1.37	1.44	1.51	V
VOLTAGE REGULATION AMPLIFIER (FB)							
FB Reference Voltage	V_{FB_REG}			1.235	1.248	1.260	V
FB Input-Leakage Current		V_{FB} = 1.3V, T_A = +25ºC		-100		+100	nA
Voltage Loop Error Amplifier Gain	G_V			1.27	1.37	1.44	mV/mV
INPUT SHORT-CIRCUIT PROTECTION (GATEN)							
External nMOSFET Gate Drive Voltage	(V_{GATEN} - V_{DCIN})			4.65	5.0	5.5	V
GATEN Drive Current	I_{GATEN}			17	20	23	µA
GATEN Active Pulldown Resistance	R_{GATEN_A}	I_{GATEN} = 100mA			1.1	2.1	Ω
GATEN Passive Pulldown Resistance	R_{GATEN_P}	$V_{EN/UVLO}$ = 0V			400	800	Ω
GATEN-DCIN Threshold	V_{GATEN_OK}			3.20	3.55	3.90	V
GATEN OK Delay	t_{GATEN_OK}				15		ms
External nMOSFET Reverse-Blocking Threshold	V_{REV}	(V_{DCIN} - V_{IN}) falling		-111	-93	-75	mV
		Hysteresis			20		
External nMOSFET Reverse-Blocking Response Time		$C_{GATEN-DCIN}$ = 10nF, V_{DCIN} < (V_{IN} - 93mV) to (V_{GATEN} - V_{DCIN}) < 2V			100	180	ns

Electrical Characteristics (continued)

(V_{IN} = V_{DCIN} = 24V, C_{VIN} = 4.7µF, C_{DCIN} = 100nF, C_{VCC} = 4.7µF, C_{VREF} = 100nF, C_{BST} = 470nF, V_{EXTVCC} = $V_{SGND/EP}$ = V_{PGND} = V_{FB} = V_{OVI} = V_{IC2} = 0V, $V_{EN/UVLO}$ = V_{LX} = V_{TMR} = V_{ILIM} = V_{CSN} = V_{CSP} = 2.5V, V_{BST} to V_{LX} = 5V, RT/SYNC = DH = DL = GATEN = COMP = $\overline{FLG}$ = ISMON = IC1 = Unconnected, T_A= -40°C to +125°C, unless otherwise noted. Typical values are at T_A= +25°C. All voltages are referenced to SGND/EP, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} to DCIN Reverse Leakage Current		V_{DCIN} = 0V, V_{IN} = 60V	$V_{EN/UVLO}$ = 0V		170	260	µA
					230	350	
CHARGER FUNCTIONS							
Constant Voltage (CV) Mode FB Threshold	V_{FB_CV}	V_{ILIM} = 1.5V, V_{FB} rising		97.15	97.50	97.85	% of V_{FB_REG}
		Hysteresis			0.3		
Overvoltage Comparator Threshold (OVI)	V_{OVI_TH}	V_{OVI} rising		1.245	1.260	1.275	V
		V_{OVI} falling		1.235	1.250	1.265	
ISMON Output-Voltage Accuracy		(V_{CSP} - V_{CSN}) = 50mV		1.41	1.50	1.59	V
		(V_{CSP} - V_{CSN}) = 10mV		0.21	0.30	0.39	
ISMON Output Resistance					90		kΩ
ISMON Output Bandwidth					100		kHz
CHARGER TIMER (TMR)							
Charger Startup Delay	t_{CH_START}	C_{TMR} = 33nF, TMR enabled			27		ms
		TMR disabled			26		
TMR Oscillator Upper Threshold	V_{TMR_H}			1.47	1.50	1.53	V
TMR Oscillator Lower Threshold	V_{TMR_L}			0.94	0.96	0.98	V
TMR Source/Sink Current	I_{TMR}			8.9	10	10.9	µA
TMR Disable Threshold	V_{TMR_DIS}	V_{TMR} > V_{TMR_DIS} (powerup check only)		1.9	2.0	2.1	V
TMR Short to SGND/EP Fault Threshold	V_{TMR_GND}	V_{TMR} < V_{TMR_GND} (powerup check only)		80	100	120	mV
Constant Current (CC) Mode Timeout	t_{FCHG}				32767		TMR CYCLES
TMR Fault Blanking Timeout	t_{BLANK_OFF}				131071		TMR CYCLES
CHARGER FAULT STATUS FLAG ($\overline{FLG}$)							
$\overline{FLG}$ Pulldown Voltage		$I_{\overline{FLG}}$ = 10mA				500	mV
$\overline{FLG}$ Leakage Current		$V_{\overline{FLG}}$ = 5.5V, T_A = +25ºC		-1		+1	µA
IC THERMAL PROTECTION							
Thermal Shutdown Threshold		Temperature rising			160		°C
		Hysteresis			10		

Note 2: Electrical specifications are production tested at T_A = +25ºC. Specifications over the entire operating temperature range are guaranteed by design and characterization.

Note 3: CC mode charging current setting is calculated using this equation:

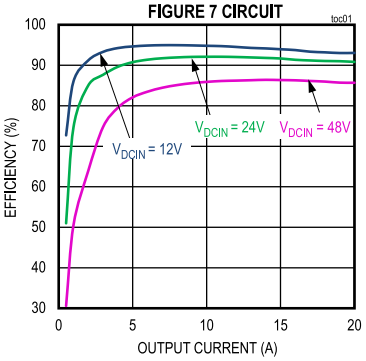
$$I_{CHGMAX} = \frac{V_{CSREG}}{R_S}$$

where R_S is the current sense resistor.

Typical Operating Characteristics

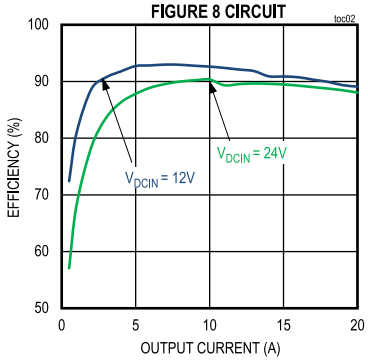
(V_{DCIN} = 24V, $V_{SGND/EP}$ = V_{PGND} = 0V, RT/SYNC = unconnected (f_{SW} = 350kHz), T_A = +25°C, unless otherwise noted. All voltages are referenced to SGND/EP, unless otherwise noted.)

EFFICIENCY vs. OUTPUT CURRENT
FIGURE 7 CIRCUIT



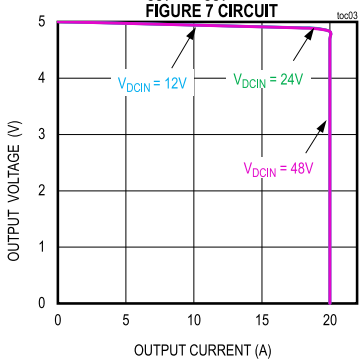
CONDITIONS: 5V OUTPUT, I_{CHGMAX} = 20A

EFFICIENCY vs. OUTPUT CURRENT
FIGURE 8 CIRCUIT



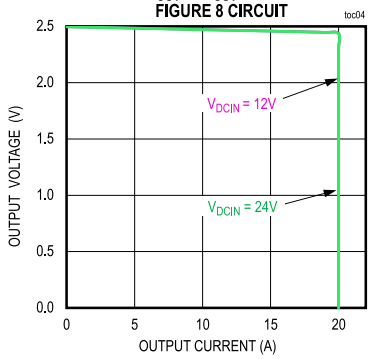
CONDITIONS: 2.5V OUTPUT, I_{CHGMAX} = 20A

V_{OUT} vs. I_{OUT} CURVE
FIGURE 7 CIRCUIT



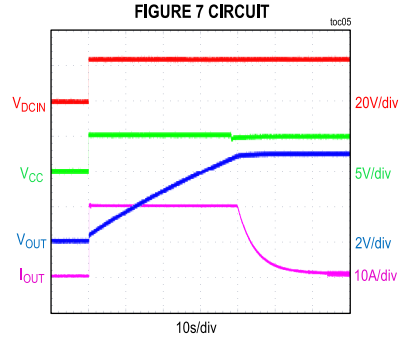
CONDITIONS: 5V OUTPUT

V_{OUT} vs. I_{OUT} CURVE
FIGURE 8 CIRCUIT



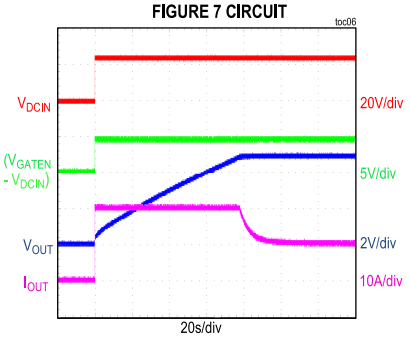
CONDITIONS: 2.5V OUTPUT

SUPERCAPACITOR CHARGING AT NO LOAD
FIGURE 7 CIRCUIT



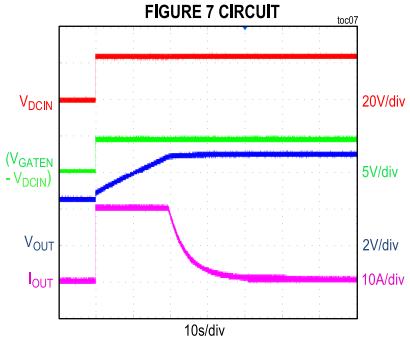
CONDITIONS: 5V OUTPUT, I_{CHGMAX} = 20A

SUPERCAPACITOR CHARGING AT 10A LOAD
FIGURE 7 CIRCUIT



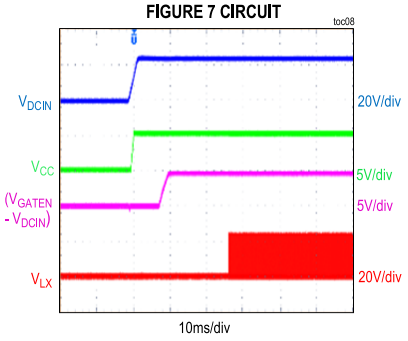
CONDITIONS: 5V OUTPUT, I_{CHGMAX} = 20A

SUPERCAPACITOR CHARGING
WITH PRE-BIASED OUTPUT OF 2.5V
FIGURE 7 CIRCUIT



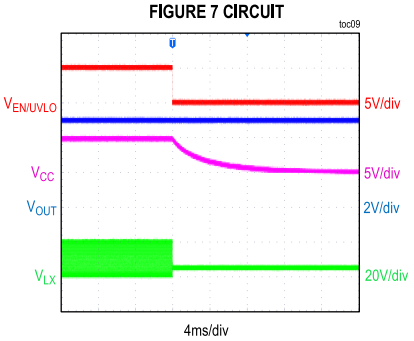
CONDITIONS: 5V OUTPUT, I_{CHGMAX} = 20A

DCIN STARTUP
FIGURE 7 CIRCUIT



CONDITIONS: 5V OUTPUT, CC MODE, I_{CHGMAX} = 20A

SHUTDOWN FROM EN/UVLO
FIGURE 7 CIRCUIT

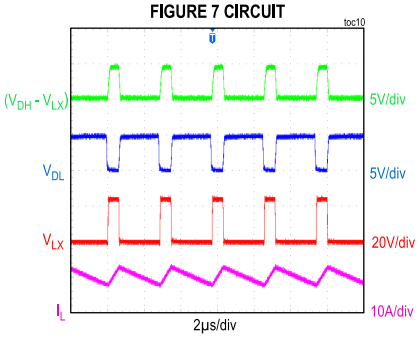


CONDITIONS: 5V OUTPUT, CV MODE, I_{CHGMAX} = 20A

Typical Operating Characteristics (continued)

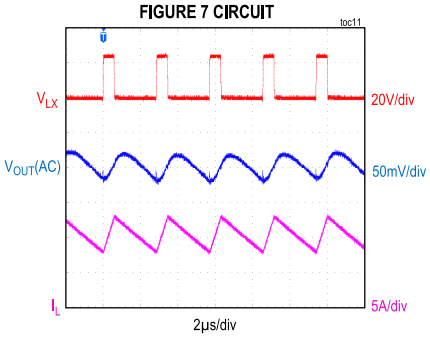
(V_{DCIN} = 24V, $V_{SGND/EP}$ = V_{PGND} = 0V, RT/SYNC = unconnected (f_{SW} = 350kHz), T_A = +25°C, unless otherwise noted. All voltages are referenced to SGND/EP, unless otherwise noted.)

STEADY-STATE SWITCHING
FIGURE 7 CIRCUIT



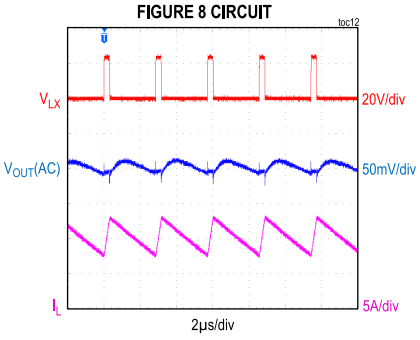
CONDITIONS: 5V OUTPUT, CV MODE, I_{LOAD} = 10A

STEADY-STATE PERFORMANCE
FIGURE 7 CIRCUIT



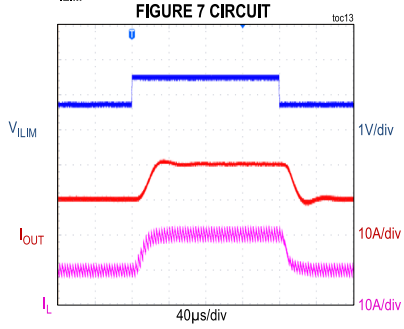
CONDITIONS: 5V OUTPUT, CV MODE, I_{LOAD} = 10A

STEADY-STATE PERFORMANCE
FIGURE 8 CIRCUIT



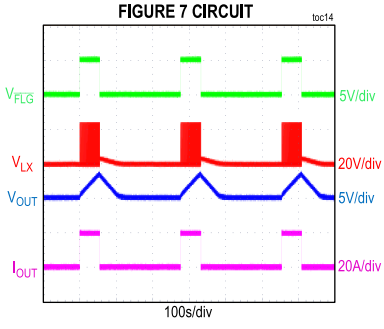
CONDITIONS: 2.5V OUTPUT, CV MODE, I_{LOAD} = 10A

ILIM TRANSIENT PERFORMANCE
V_{ILIM} IS VARIED BETWEEN 0.75V AND 1.5V
FIGURE 7 CIRCUIT



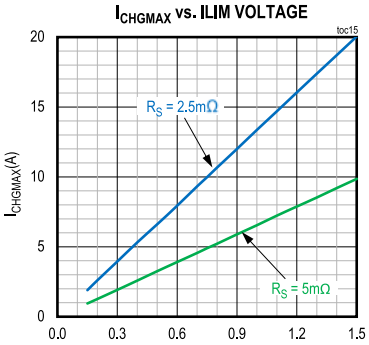
CONDITIONS: CC MODE

TIMER FAULT AND RECOVERY
FIGURE 7 CIRCUIT



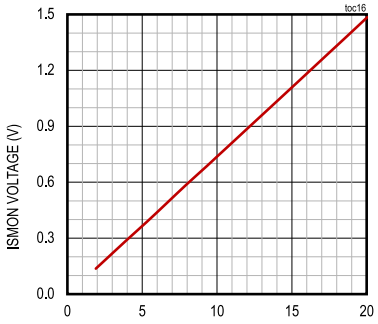
CONDITIONS: 5V OUTPUT, CC MODE, I_{LOAD} = 10A, T_{TMR} = 55s, I_{CHGMAX} = 20A

I_{CHGMAX} vs. ILIM VOLTAGE



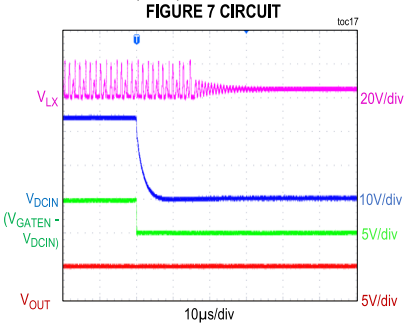
CONDITIONS: CC MODE

ISMON VOLTAGE vs. OUTPUT CURRENT



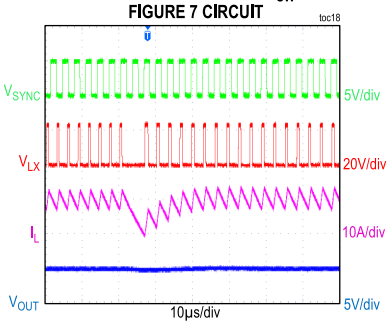
CONDITIONS: CC MODE

INPUT (DCIN) SHORT PROTECTION
FIGURE 7 CIRCUIT



CONDITIONS: 5V OUTPUT, CV MODE

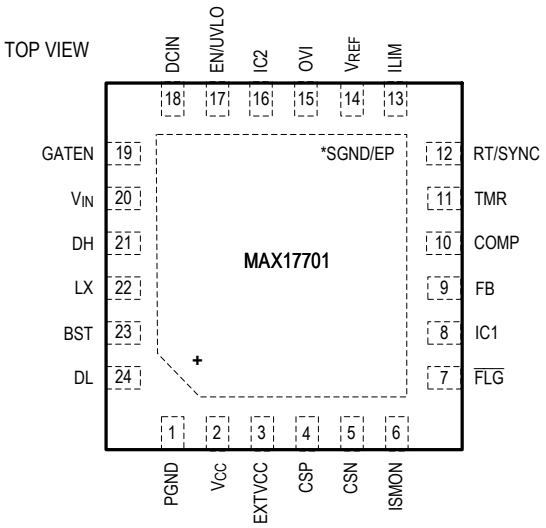
EXTERNAL CLOCK SYNCHRONIZATION
AFTER 112 CYCLES OF f_{SW}
FIGURE 7 CIRCUIT



CONDITIONS: 5V OUTPUT, CV MODE, I_{LOAD} = 10A, I_{CHGMAX} = 20A, f_{SW} = 350kHz, f_{SYNC} = 315kHz

Pin Configuration

MAX17701



24-PIN TQFN
4mm x 4mm

Pin Description

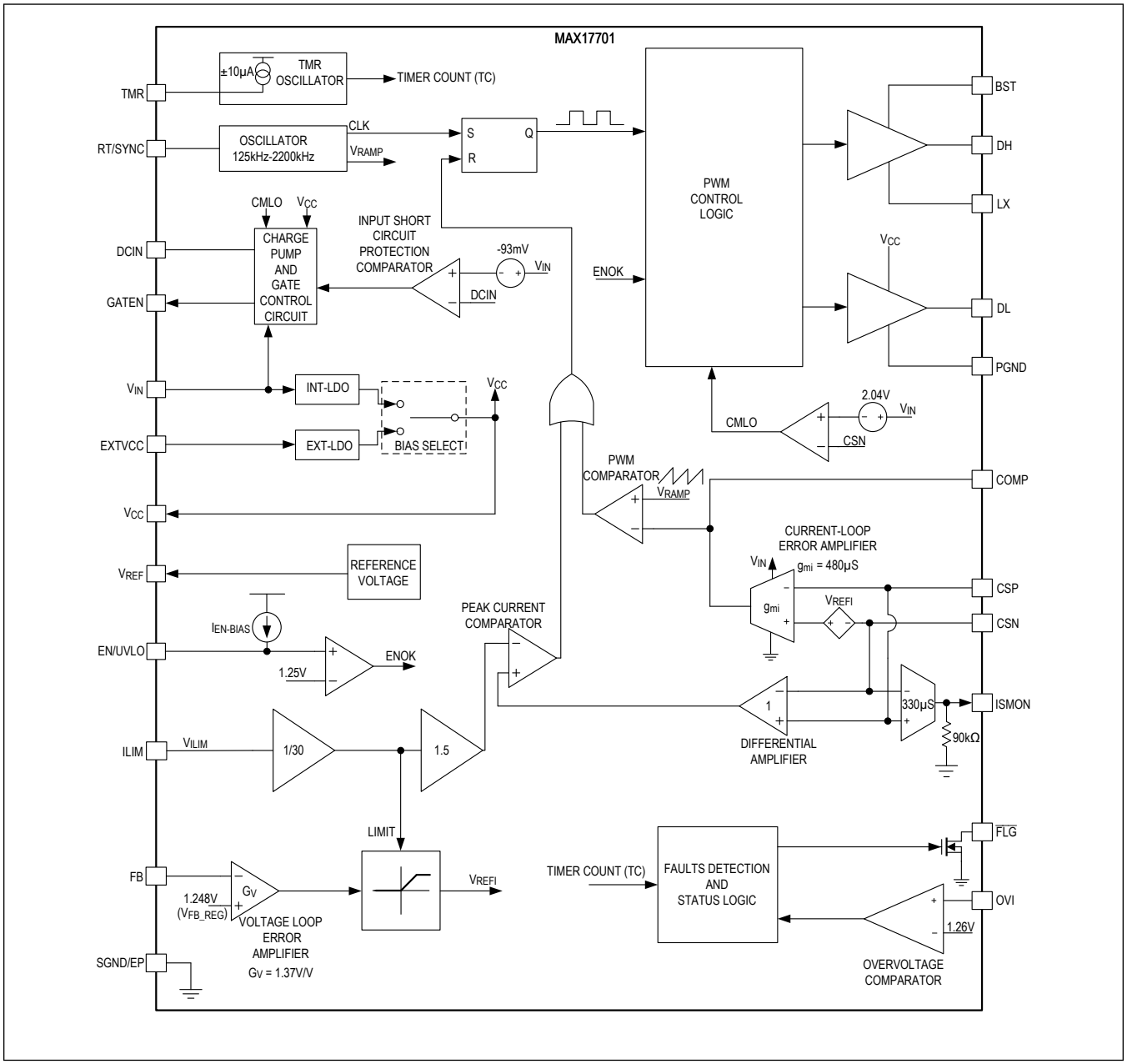
PIN	NAME	FUNCTION
1	PGND	Power Ground. Connect to the return terminal of a V_{CC} bypass capacitor placed close to IC, and the source terminal of external low-side nMOSFET. Refer to the MAX17701 EV kit data sheet for a PCB layout example.
2	V_{CC}	Internal LDO Output. Connect a minimum of 4.7µF/0805, low-ESR ceramic capacitor between V_{CC} and PGND. V_{CC} supports the IC internal control circuitry and gate drive current for external nMOSFETs.
3	EXTVCC	External Power-Supply Input for EXT-LDO. To power internal circuitry from an external supply, apply a voltage between 4.8V and 24V to the EXTVCC pin. Connect a minimum of 1µF/0603, low-ESR ceramic capacitor between EXTVCC and SGND/EP. Leave EXTVCC open when not used.
4	CSP	Inverting Input of the Current Loop Error Amplifier. The CSP and CSN pins measure the voltage across the current sense resistor R_S (see Figure 4).
5	CSN	Non-Inverting Input of the Current Loop Error Amplifier. Connect CSN to the node connecting the output capacitor and current sense resistor R_S. Use Kelvin connections and route the CSP and CSN traces as a differential pair (see Figure 4).
6	ISMON	Output of Charging Current Monitor. Bypass ISMON with a 1nF low-ESR ceramic capacitor to SGND/EP. The voltage on this pin is 30 times the voltage drop across the current sense resistor R_S.
7	$\overline{FLG}$	Open Drain Fault Status Output. The $\overline{FLG}$ pin is pulled low when either the safety timer times out or when there is a hardware fault. See the *Fault Status Output ($\overline{FLG}$)*, *Hardware Faults* sections for more details.
8	IC1	Internal Connection. Connect to SGND/EP.
9	FB	Feedback Input. Connect FB to the center node of a resistor-divider from the positive terminal of supercapacitor to SGND/EP to set the output voltage. See the *Setting the Output Voltage and Voltage Regulation Loop (FB)* section for more details.

Pin Description (continued)

PIN	NAME	FUNCTION
10	COMP	Current Loop Error Amplifier Output. Connect a compensation network at this pin to stabilize the inner current loop. See the *Current Regulation Loop Compensation (COMP)* section for more details.
11	TMR	Supercapacitor Safety Timer Setting Pin. A capacitor from TMR to SGND/EP sets the charging time in CC mode. Place the timer capacitor close to the TMR pin. Connect TMR to V_{REF} to disable the timer function. See the *Charger Timers (TMR)* section for more details.
12	RT/SYNC	Switching Frequency Programming/Synchronization Input. Connect a resistor from RT/SYNC to SGND/EP to set the switching frequency between 125kHz to 2.2MHz. Leave RT/SYNC open for the default 350kHz frequency. See the *Setting the Switching Frequency and External Clock Synchronization (RT/SYNC)* section for more details.
13	ILIM	CC Mode Charging Current Programming Input. Connect ILIM to the center node of a resistor divider between V_{REF} and SGND/EP to set the CC mode charging current. Connect to V_{REF} for default CC mode charging current setting. See the *CC Mode Charging Current Setting (ILIM)* section for more details.
14	V_{REF}	2.5V Reference Output. Bypass V_{REF} with a 0.1µF low-ESR ceramic capacitor to SGND/EP. See the *Reference Voltage (V_{REF})* section for more details.
15	OVI	Overvoltage Detection Input. Connect OVI to the center node of a resistor divider from the output voltage node to SGND/EP. If V_{OVI} exceeds V_{OVI_TH}, charging is stopped and the charger enters into the latched fault.
16	IC2	Internal Connection. Connect to SGND/EP
17	EN/UVLO	Enable/Undervoltage Lockout Input. Connect to the center node of a resistor divider between DCIN and SGND/EP to set the input voltage at which the device turns on. Connect to SGND/EP to shutdown the device. See the *Setting the Input Undervoltage-Lockout Level (EN/UVLO)* section for more details.
18	DCIN	Input Supply Voltage Sense Pin. Bypass DCIN with a 0.1µF ceramic capacitor to PGND. Refer to the MAX17701 EV kit data sheet for the recommended PCB layout and routing.
19	GATEN	Gate Drive Output for External nMOSFET. GATEN controls the gate of an external nMOSFET connected between DCIN and V_{IN} to prevent supercapacitor discharge when DCIN is shorted to PGND. See the *Input Short Circuit Protection (GATEN)* section for more details.
20	V_{IN}	MAX17701 IC Supply Pin. Bypass V_{IN} to PGND with a 0.1µF ceramic capacitor. Refer to the MAX17701 EV kit data sheet for the recommended PCB layout and routing.
21	DH	High Side nMOSFET Gate Driver Output. Connect to the gate of a high-side nMOSFET.
22	LX	Switching Node Connection Input. Connect to the switching node of the converter.
23	BST	Bootstrap Capacitor Connection Input. Connect a 0.1µF (min) capacitor between the BST and LX pins. See the *Bootstrap Capacitor Selection (BST)* section for more details.
24	DL	Low-Side nMOSFET Gate Driver Output. Connect to the gate of a low-side nMOSFET.
—	SGND/EP	Signal Ground, Exposed Pad. Refer to the MAX17701 EV kit data sheet recommended method for the PCB layout, routing, and thermal vias.

Functional Diagrams

Block Diagram



Detailed Description

The MAX17701 is a 4.5V to 60V, synchronous, step-down, supercapacitor charger controller designed to operate over a -40°C to +125°C temperature range. It charges a supercapacitor with constant charging current with up to ±4% accuracy. After the supercapacitor is charged, the device regulates the no load output voltage with ±1% accuracy. The MAX17701 supports a wide output-voltage range of 1.25V to (V_{DCIN} - 4V).

The MAX17701 features a constant frequency, average current-mode control architecture shown in Figure 1. An internal current loop consists of a transconductance amplifier g_{mi} that senses the inductor current flowing through current sense resistor R_S as a voltage drop across the CSP and CSN pins. The current sense voltage is compared with a current loop reference voltage (V_{REFI}), which is set by the outer voltage loop error amplifier (G_V) and limited by the voltage programmed at the ILIM pin (V_{ILIM}). The voltage at the COMP pin is compared with a 1.44V (typ) ramp using a PWM comparator to set the duty cycle of the converter. The required compensation to stabilize the current loop is applied at the COMP pin using R_Z, C_Z, and C_P. Under steady-state conditions, the inner current loop forces the voltage drop across R_S equal to V_{REFI}.

The output voltage is monitored by the voltage error amplifier G_V with a resistor divider (R_{TOP}, R_{BOT}) connected across the positive and negative supercapacitor terminals with the center node connected to the FB pin. The voltage at the FB pin (V_{FB}) is compared with the FB reference voltage (V_{FB_REG}). The voltage loop error amplifier sets the current loop reference voltage (V_{REFI}). V_{REFI} is limited to $\frac{V_{ILIM}}{30}$ until $V_{FB} \le \left[V_{FB\_REG} - \frac{V_{ILIM}}{30 \times G_V}\right]$. This results in a constant current through R_S. When the output voltage rises, such that $V_{FB} > \left[V_{FB\_REG} - \frac{V_{ILIM}}{30 \times G_V}\right]$, V_{REFI}; hence, the output load current (I_{LOAD}) proportionately reduces. The steady-state FB regulation voltage, and consequently the output voltage depend on the load (I_{LOAD}) connected across the supercapacitor, as given by the following equation:

$$V_{OUT\_LOAD} = \left[V_{FB\_REG} - \frac{I_{LOAD} \times R_S}{G_V}\right] \times \left[\frac{R_{TOP} + R_{BOT}}{R_{BOT}}\right]$$

where,

V_{FB_REG} = FB reference voltage

V_{OUT_LOAD} = Steady-state output voltage for a given load current

I_{LOAD} = Output load current of the charger

R_{TOP}, R_{BOT} = Output voltage feedback voltage divider resistors

G_V = Voltage loop error amplifier gain (1.37V/V)

The MAX17701 provides input short-circuit protection, and prevents supercapacitor discharging for input supply-side short-circuit events by means of an external nMOSFET. A safety timer (TMR) sets the maximum allowed CC mode charging time to improve system safety. The device features an uncommitted comparator, which can be used to detect an output overvoltage (OVI), which improves the safety of load circuitry, and prevents the supercapacitor from overcharging.

The switching frequency of the device can be programmed from 125kHz to 2.2 MHz using a resistor at the RT/SYNC pin. The RT/SYNC also provides an external clock synchronization feature. Input undervoltage lockout is implemented using the EN/UVLO pin. An open-drain $\overline{FLG}$ output indicates faults. The system current can be monitored using the ISMON pin.

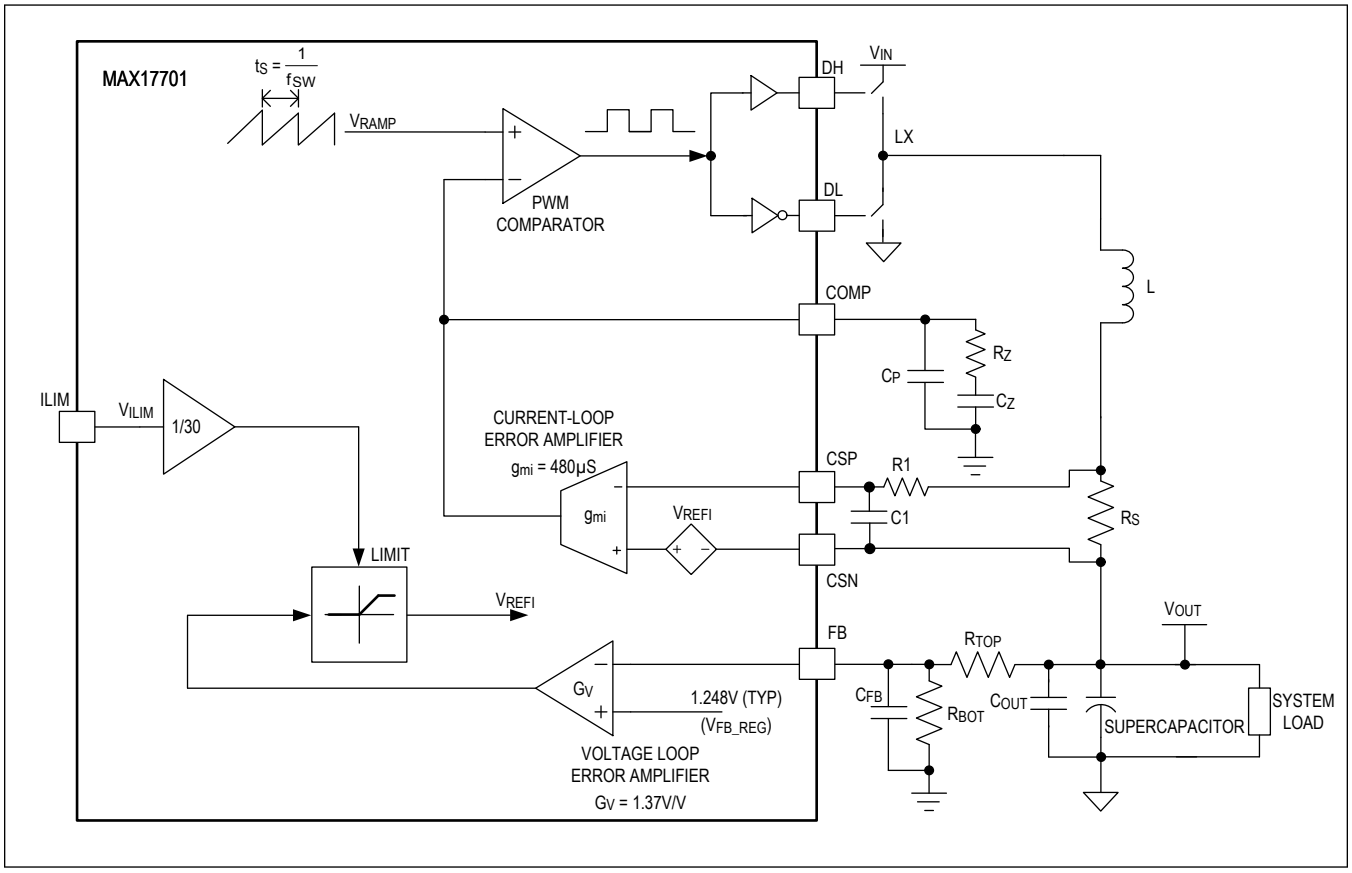


Figure 1. Average Current Mode Control Loop

Power-Up/-Down Sequence

Figure 2 shows the MAX17701 power-up/-down sequence when DCIN voltage is applied/removed. When DCIN voltage reaches a level such that $V_{EN/UVLO}$ is around 0.7V (V_{ENT}) the INT-LDO regulator is enabled and V_{CC} rises. When V_{CC} rises above 4.2V (V_{CC-UVR}) and $V_{EN/UVLO}$ rises above 1.25V ($V_{EN\_TH\_R}$), the MAX17701 initiates EN/UVLO debounce and checks for hardware faults. If there are no hardware faults (see the *Hardware Faults* section) detected at power-up, the MAX17701 enables internal blocks during charger startup delay time t_{CH_START}. After this delay, the charger initiates LX switching and enters CC mode. In CC mode, the current is regulated at the CC mode charging current setting (I_{CHGMAX}). The safety timer counts the charging time in CC mode and if the output voltage reaches constant voltage mode ($V_{FB} > V_{FB\_CV}$) within the safety timer setting (t_{SC_TMR}), the charger enters constant voltage (CV) mode and continues to operate.

When $V_{EN/UVLO}$ falls below 1.09V ($V_{EN\_TH\_F}$), the MAX17701 initiates a shutdown sequence with a debounce time of 2ms (typ). If the input voltage decreases such that V_{IN} - V_{CSN} falls below the current loop error amplifier undervoltage lockout falling threshold 1.95V (V_{CMUVLO}), the COMP is pulled low immediately, and the MAX17701 initiates a shutdown sequence with a debounce time of 100µs (typ). The converter stops switching, and GATEN is pulled down with 1.1Ω (R_{GATEN_A}) to DCIN to turn off the external nMOSFET.

If $V_{EN/UVLO}$ falls below 0.64V (V_{ENT}), the MAX17701 initiates a shutdown sequence with a debounce time of 10µs (typ). During this shutdown sequence, the MAX17701 pulls down the GATEN with 400Ω (R_{GATEN_P}) to DCIN to turn off the external nMOSFET. See the *Setting the Input Undervoltage-Lockout Level (EN/UVLO)* section for more details.

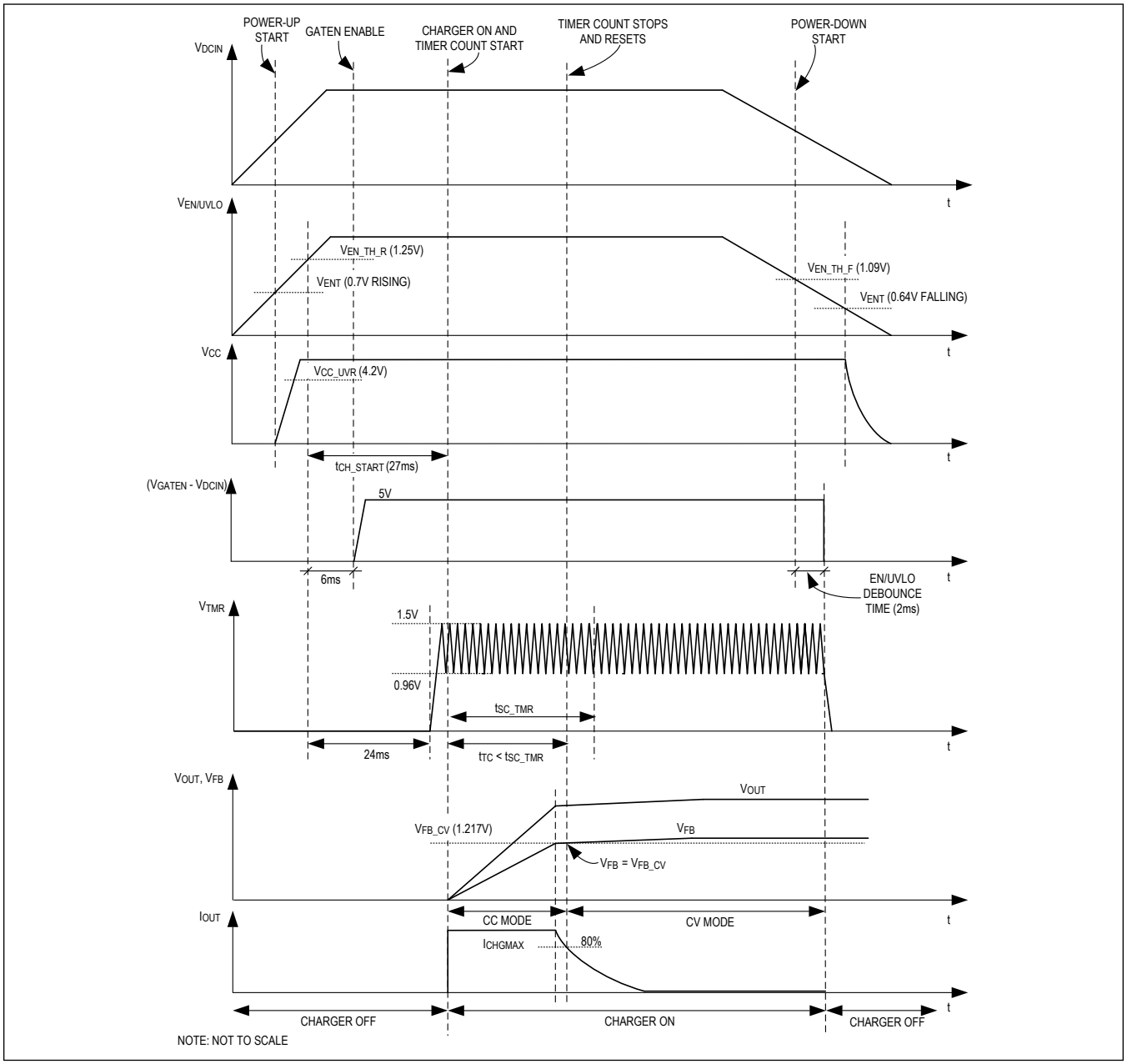


Figure 2. Charger Power-Up/-Down Sequence

Input Short-Circuit Protection (GATEN)

The MAX17701 provides gate drive output (GATEN) that drives a logic-level gate threshold external nMOSFET, which turns off and prevents supercapacitor discharging for input supply short-circuit events. The GATEN is pulled up with 20µA (I_{GATEN}) when V_{IN} is 2.04V (V_{CMUVLO}) above V_{CSN}. If V_{GATEN} does not reach 3.55V (V_{GATEN_OK}) within 15ms (t_{GATEN_OK}), MAX17701 enters latched hardware fault.

Figure 3 depicts the MAX17701 behavior when DCIN is shorted to PGND. When V_{DCIN} is 93mV (V_{REV}) below V_{IN},

GATEN is pulled down with 1.1Ω (R_{GATEN_A}) and the external nMOSFET is turned off within 100ns (typ). When $V_{EN/UVLO}$ goes below 0.64V (V_{ENT}), the MAX17701 shuts down with 10µs (typ) debounce time. When DCIN-to-PGND short is removed, the power-up sequence is initiated (see the *Power-Up/Down Sequence* section). When the input short-circuit protection is not used, connect a 1nF capacitor between GATEN and DCIN, and short DCIN to V_{IN}.

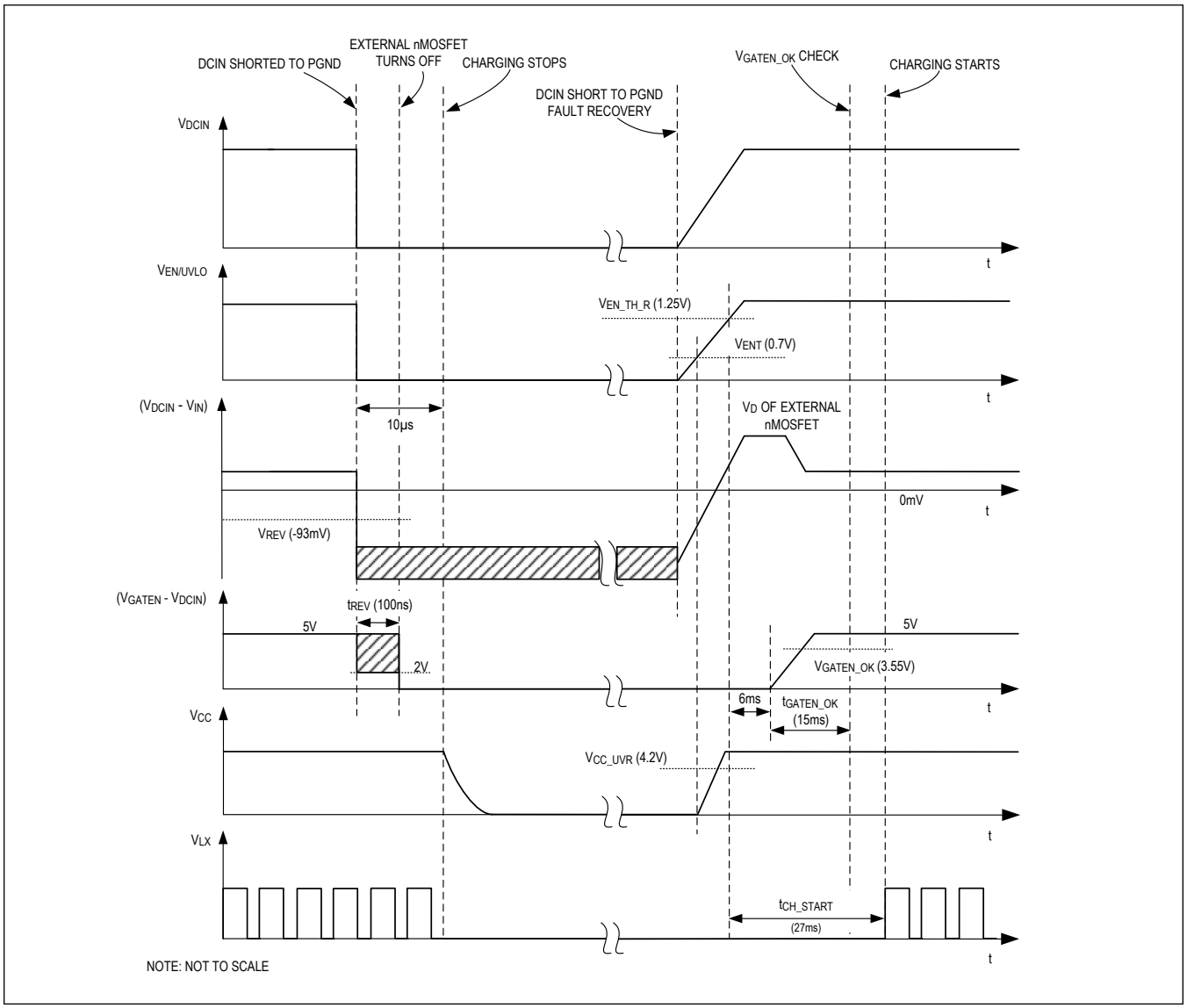


Figure 3. Input Short-Circuit Protection and Recovery Timing Diagram

Charger Operation

MAX17701 offers constant current (CC) mode and constant voltage (CV) mode for charging a supercapacitor. In CC mode, the charging current is regulated to the CC mode charging current (I_{CHGMAX}) proportional to V_{ILIM}. The safety timer starts counting when the device enters CC mode. When V_{FB} goes above 1.217V (V_{FB_CV}) within the CC mode timeout period (t_{SC_TMR}), the charger enters CV mode and the safety timer stops counting (see *Charger Timers (TMR)* section). The safety timer count resets when the device enters CV mode. In CV mode, the device continues to charge

the supercapacitor until V_{FB} reaches 1.248V (V_{FB_REG}). The charger regulates V_{FB} at V_{FB_REG} at no load. When V_{FB} drops below 1.213V (V_{FB_CV}), the charger exits CV mode, enters CC mode, and the timer count restarts.

Charger Timers (TMR)

The MAX17701 offers a programmable timer feature to provide additional safety to the supercapacitor and the connected load. Connect a capacitor from TMR to SGND/EP to enable the timer feature. Connect TMR to V_{REF} to disable the timer feature. The timer counts the charging time in CC mode. If V_{FB} does not reach 1.217V (V_{FB_CV}) within CC mode timeout period (t_{SC_TMR}), the charger turns off. The charger restarts after 4 times t_{SC_TMR}. The MAX17701 supports 130pF to 12µF capacitance on TMR, translating into a CC mode timeout period range of 1 second to 12 hours.

The safety timer is programmed based on supercapacitor value (C_{SUP}), output voltage (V_{OUT}), and CC mode charging current setting (I_{CHGMAX}). Refer to the *CC Mode Charging Current Setting (ILIM)* section.

Choose the required safety timer period using the following equation:

$$t_{SC\_TMR} \geq \frac{C_{SUP} \times V_{OUT}}{I_{CHGMAX} - I_{LOAD}}$$

where I_{LOAD} is the system load during the supercapacitor charging period

Select $I_{CHGMAX} \geq 1.5 \times I_{LOAD}$ to ensure the charger enters CV mode

Use the following equation to calculate C_{TMR} for the required t_{SC_TMR}:

$$C_{TMR} = \left(\frac{t_{SC\_TMR}}{2 \times t_{FCHG}} - 8 \times 10^{-6}\right) \times \left(\frac{I_{TMR}}{V_{TMR\_H} - V_{TMR\_L}}\right)$$

where

t_{SC_TMR} = Desired safety timer timeout setting in seconds

C_{TMR} = TMR capacitor in Farad

t_{FCHG} = Number of TMR cycles in CC mode (32767)

V_{TMR_H} = TMR oscillator upper threshold (1.5V)

V_{TMR_L} = TMR oscillator lower threshold (0.96V)

I_{TMR} = TMR pin source/sink current (10µA)

Fault Status Output ($\overline{FLG}$)

The MAX17701 features an open drain fault status output pin ($\overline{FLG}$) to indicate the status of the charger. Connect a 10kΩ external pullup resistor from V_{CC} to $\overline{FLG}$. $\overline{FLG}$ goes high (high-impedance) when MAX17701 is in normal operation (no faults). $\overline{FLG}$ goes low when the safety timer times out or when a hardware fault is detected.

Hardware Faults

The MAX17701 features hardware fault checks at power-up and during normal operation. Table 1 provides various fault detection features available and their behaviours in MAX17701.

Table 1. Protection Under System Faults

FAULT CONDITION	FAULT MONITOR STATE	FAULT BEHAVIOR
RT/SYNC to SGND/EP short	Powerup check	Latched fault, need to recycle power or EN/UVLO to restart the device
GATEN to DCIN short		
TMR pin left unconnected		
TMR to SGND/EP short		
V_{REF} to SGND/EP short		
Output overvoltage ($V_{OVI} > V_{OVI\_TH}$)		

Table 1. Protection Under System Faults (continued)

FAULT CONDITION	FAULT MONITOR STATE	FAULT BEHAVIOR
(V_{GATEN} - V_{DCIN}) < V_{GATEN_OK}	Continuous, during normal operation	
V_{REF} < 2.36V or V_{REF} > 2.64V		
Output overvoltage (V_{OVI} > V_{OVI_TH})		

Linear Regulator (V_{CC} and EXTVCC)

The MAX17701 integrates two internal low-dropout (LDO) linear regulators INT-LDO and EXT-LDO that power V_{CC}. V_{CC} powers gate drivers and internal control circuitry. INT-LDO is powered from V_{IN} and turns on when $V_{EN/UVLO}$ > V_{ENT} (0.7V). EXT-LDO is powered from EXTVCC. At any time, only one of these two linear regulators operates, depending on the EXTVCC voltage. If V_{EXTVCC} > 4.7V (typ) then V_{CC} is powered from EXT-LDO. If V_{EXTVCC} < 4.46V(typ), then V_{CC} is powered from INT-LDO. Powering V_{CC} from EXTVCC reduces on-chip dissipation and increases efficiency at higher input voltages. EXTVCC should be connected to V_{OUT} for applications with V_{OUT} > 4.7V (typ). The maximum voltage limit on EXTVCC is 24V. Bypass EXTVCC with a 1µF ceramic capacitor to SGND/EP. Leave EXTVCC open when not used. Bypass V_{CC} to PGND with at least a 4.7µF/0805 (GRM21BR71C475KE51), low-ESR ceramic capacitor.

Reference Voltage (V_{REF})

The MAX17701 provides a 2.5V reference voltage on the V_{REF} pin with ±1.4% accuracy. V_{REF} can be used to program V_{ILIM} to set the CC mode charging current (I_{CHGMAX}). Connect a minimum 0.1µF low-ESR ceramic capacitor between V_{REF} and SGND/EP. See the *CC Mode Charging Current Setting (ILIM)* section for more details.

Setting the Switching Frequency and External Clock Synchronization (RT/SYNC)

The switching frequency of the device can be programmed from 125kHz to 2.2MHz by using a resistor ($R_{RT/SYNC}$) connected from the RT/SYNC pin to SGND/EP. $R_{RT/SYNC}$ can be calculated using the following equation:

$$R_{RT/SYNC} = \frac{44830}{f_{SW}} - 1.205$$

Where $R_{RT/SYNC}$ is in kΩ and f_{SW} is in kHz. Leave the RT/SYNC pin unconnected to operate the device at 350kHz default switching frequency.

The MAX17701 can be synchronized to an external clock coupled to the RT/SYNC pin through a 10pF ceramic capacitor. The external clock is detected after checking the rising edge for 112 cycles of the internal clock (set by RT/SYNC). If the external clock frequency is within the allowed SYNC frequency range (±10% of nominal internal clock frequency), the device stops switching for 2 switching time periods and then restarts with an external clock. When the external clock is removed, the device stops switching for 10 switching time periods and then restarts with an internal clock.

The minimum external clock pulse-width should be greater than 100ns. The off-time duration of the external clock should be at least 100ns.

Peak Current-Limit

The MAX17701 provides a cycle-by-cycle overcurrent protection by limiting the peak current-sense voltage (V_{CSP} - V_{CSN}) across the current sense pins. When an overcurrent event is detected, the overcurrent comparator in the MAX17701 terminates the DH pulse and limits the peak current. The overcurrent fault is not latched.

Charging Current Monitoring (ISMON)

The output charge current can be monitored by observing the voltage at the ISMON pin. Connect a 1nF ceramic capacitor on ISMON to filter out the switching frequency component in the ISMON voltage. The charging current is given by the following equation:

$$I_{CHG} = \frac{V_{ISMON}}{30 \times R_S}$$

where,

I_{CHG} = Charging current

V_{ISMON} = Voltage at the ISMON pin

R_S = Current-sense resistance

Thermal-Shutdown Protection

Thermal-shutdown protection limits junction temperature of the device. When the junction temperature of the device exceeds +160ºC, an on-chip thermal sensor shuts down the device, allowing the device to cool. The device turns on after the junction temperature reduces by 10ºC. Carefully evaluate the total power dissipation to avoid unwanted triggering of the thermal shutdown during normal operation (see the *Power Dissipation* section).

Applications Information

Inductor Selection

Three key inductor parameters must be specified for operation with the device: inductance value (L), DC resistance (R_{DCR}), and inductor saturation current (I_{SAT}).

The required inductance is calculated based on the inductor current ripple ratio (LIR), i.e., ratio of peak-to-peak ripple current (ΔI_L) to CC mode charging current (ICHGMAX). A good compromise between size and loss is an LIR of 0.3.

The switching frequency, CC mode charging current, input voltage, and output voltage determine the inductor value as follows:

$$L = \frac{V_{OUT} \times (1-D)}{LIR \times I_{CHGMAX} \times f_{SW}}$$

where:

V_{OUT} = Desired voltage across supercapacitor

I_{CHGMAX} = CC mode charging current

D = Duty cycle of the converter, V_{OUT}/V_{IN}

V_{IN} = Nominal input voltage

f_{SW} = Switching frequency

Select an inductor that is nearest to the calculated value. The inductor RMS-current rating should be more than the CC mode charging current. Select a low-loss inductor with acceptable dimensions and the lowest possible DC resistance. The saturation current rating (I_{SAT}) of the inductor must be high enough to ensure that saturation can occur only above the overcurrent threshold corresponding to V_{CSPEAK}.

Output Capacitor Selection

Supercapacitors have significant equivalent series resistance (ESR_{SUP}). The switching ripple component of charger output current flows into this ESR_{SUP} and results in a large output-voltage ripple. To reduce the voltage ripple across the supercapacitor, additional X7R ceramic capacitors and/or low-ESR POSCAP capacitors can be used at the output of the charger.

X7R ceramic output capacitors are preferred due to their stability over temperature in industrial applications. For higher values of output capacitance, low-ESR POSCAP capacitors can be used in parallel with ceramic capacitors.

Calculate the required output capacitance (C_{OUT}) based on the following equation:

$$C_{OUT} = \frac{25 \times I_{CHGMAX}}{f_{SW} \times V_{OUT}}$$

where:

I_{CHGMAX} = CC mode charging current setting

f_{SW} = Switching frequency

V_{OUT} = Desired voltage across the supercapacitor

Derating of ceramic capacitors with DC-bias voltage must be considered while selecting the capacitors, using the manufacturer data sheet. The selected output capacitor C_{OUT_SEL} and its equivalent series resistance (ESR_{COUT}) affect the output-voltage ripple (ΔV_{OUT}). Estimate the resultant ΔV_{OUT} using the following equation:

$$\Delta V_{OUT} \approx \Delta I_L \times \left(ESR_{COUT} + \frac{1}{8 \times f_{SW} \times C_{OUT\_SEL}} \right)$$

where ΔI_L is the inductor peak-to-peak ripple current.

Input Capacitor Selection

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the switching converter. Calculate the required input capacitance at V_{IN} (C_{VIN}) using the following equation:

$$C_{VIN} = \frac{I_{CHGMAX} \times D \times \left(1 - D\right)}{\eta \times f_{SW} \times \Delta V_{IN}}$$

where:

$D = \frac{V_{OUT}}{V_{IN}}$ is the duty ratio of the converter

f_{SW} = Switching frequency

ΔV_{IN} = Allowable input-voltage ripple

η = Efficiency of the converter

I_{CHGMAX} = CC mode charging current

Choose $\Delta V_{IN} \leq 0.5V$ to minimize voltage ripple across the external nMOSFET and to provide robust operation during input short-circuit events.

The input capacitor RMS current (I_{RMS}) is calculated using the following equation:

$$I_{RMS} = I_{CHGMAX} \times \frac{\sqrt{V_{OUT} \times [V_{IN} - V_{OUT}]}}{V_{IN}}$$

Choose low-ESR ceramic input capacitors that exhibit less than a +10°C temperature rise at I_{RMS} for optimal long-term reliability. X7R capacitors are recommended in industrial applications for their temperature stability. Derating of ceramic capacitors with DC-bias voltage must be considered while selecting the capacitors using the manufacturer data sheet.

Choose an electrolytic capacitor at DCIN in order to prevent the DCIN voltage from being less than -0.3V during input short events. An electrolytic capacitor also provides the damping for potential oscillations caused by inductance of the longer input power path and input ceramic capacitor (C_{VIN}). Additionally, if required, add a Schottky diode at DCIN in parallel with the electrolytic capacitor.

Operating Input-Voltage Range

The following equations are used to calculate the operating input-voltage range for a given output voltage and CC mode charging current setting. The minimum operating input voltage on the DCIN pin is given by the higher value from the two calculated voltages:

$$V_{DCIN(MIN1)} = \frac{V_{OUT} + I_{CHGMAX} \times \left(R_{DS\_ON(LS)} + R_{DCR(MAX)}\right)}{\left(1 - \left(2.1 \times f_{SW} \times \left(t_{DT\_HL} + t_{MIN\_ON\_DL(MAX)}\right)\right)\right)} + I_{CHGMAX} \times \left(R_{DS\_ON(HS)} - R_{DS\_ON(LS)}\right)$$

$V_{DCIN(MIN2)} = 1.15 \times (V_{OUT} + 3V)$

where:

$V_{DCIN(MIN1)}$, $V_{DCIN(MIN2)}$ = Minimum operating input voltages; the higher of the two values is the minimum operating input voltage ($V_{DCIN(MIN)}$)

V_{OUT} = Desired regulation voltage across the supercapacitor

I_{CHGMAX} = CC mode charging current setting

f_{SW} = Switching frequency in Hz

$R_{DCR(MAX)}$ = Worst-case DC resistance of the inductor in Ω

$R_{DS\_ON(HS)}$, $R_{DS\_ON(LS)}$ = Worst-case on-state resistances of high-side and low-side internal MOSFETs in Ω,

respectively

t_{DT_HL} = Dead time (30ns)

$t_{MIN\_ON\_DL(MAX)}$ = Worst-case DL minimum controlled on-time (100ns).

The maximum operating input voltage on the DCIN pin is calculated as follows:

$$V_{DCIN(MAX)} = \frac{V_{OUT}}{\left(1.05 \times f_{SW} \times t_{MIN\_ON\_DH(MAX)}\right)}$$

where $t_{MIN\_ON\_DH(MAX)}$ is the worst-case DH minimum controlled on-time (100ns).

CC Mode Charging Current Setting (ILIM)

The CC mode charge current setting involves setting up a voltage on the ILIM pin (V_{ILIM}) and choice of current sense resistor R_S. Selection of R_S involves a trade-off between power loss and charging current accuracy. The best MAX17701 charging current accuracy is obtained with a voltage drop (V_{CSP} - V_{CSN}) of 50mV across R_S. (V_{CSP} - V_{CSN}) can be reduced at the expense of the charging current accuracy to reduce power loss. The recommended range for voltage across R_S is 25mV (±8% charging current accuracy) to 50mV (±4% charging current accuracy). R_S can be calculated using the following equation:

$$R_S = \frac{\left(V_{CSP} - V_{CSN}\right)}{I_{CHGMAX}}$$

Once R_S is selected, V_{ILIM} can be calculated using the following equation:

$$V_{ILIM} = 30 \times R_S \times I_{CHGMAX}$$

A resistor divider from V_{REF} to SGND/EP can be used to program V_{ILIM}, as shown in Figure 4. The resistor-divider values are calculated as follows:

$$R_{LIM1} = 20 \times \left(V_{REF} - V_{ILIM}\right)k\Omega$$

$$R_{LIM2} = 20 \times V_{ILIM}k\Omega$$

The permitted voltage range for the V_{ILIM} setting is 0.15V to 1.5V. The MAX17701 can be set to the default I_{CHGMAX} setting corresponding to (V_{CSP} - V_{CSN}) = 50mV across R_S by connecting ILIM to V_{REF}.

Connect an R-C filter in the current-sense signal path as shown in Figure 4 to attenuate switching noise while preserving accuracy and bandwidth. The R-C filter corner frequency should be 5 times the switching frequency. The recommended filter resistance (R1) is 40Ω for minimal impact on the current-sense accuracy. The filter capacitor C1 should be placed close to the CSP and CSN pins. Calculate the value of filter capacitor C1 using the following equation:

$$C1 = \frac{1}{2\pi x R1 x 5 x f_{SW}}$$

where f_{SW} = Switching frequency

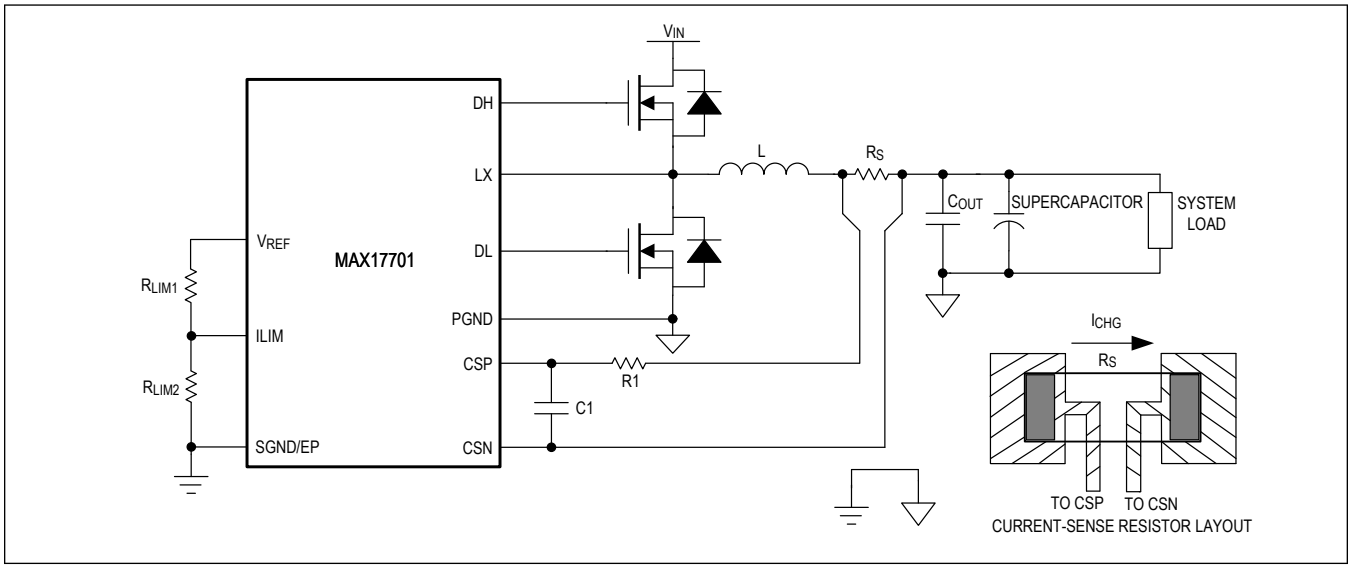


Figure 4. Current-Sense Circuit

Setting the Input Undervoltage-Lockout Level (EN/UVLO)

The MAX17701 offers an adjustable input undervoltage-lockout level using the EN/UVLO pin. Pulling the EN/UVLO pin below 1.09V (typ) stops charger operation. Pulling EN/UVLO below 0.64V (typ) causes the MAX17701 to shut down. In this state, the device draws I_{IN-SH} (7µA) quiescent current. Figure 5 shows the recommended EN/UVLO configuration based on the required input-voltage range.

Connect EN/UVLO to the center node of a resistor divider from the DCIN to SGND/EP to set the input voltage at which the device turns on. Choose R1 as follows:

$R1 \le (10000 \times V_{DCIN(MIN)})$

where $V_{DCIN(MIN)}$ is the voltage at which the device is required to turn on.

Calculate the value of R2 using the following equation:

$$R2 = \frac{V_{EN\_TH\_R} \times R1}{(V_{DCIN(MIN)} - V_{EN\_TH\_R} + (I_{EN-BIAS} \times R1))}$$

where:

$I_{EN-BIAS}$ = Internal bias pullup current on the EN/ULVO pin

$V_{EN\_TH\_R}$ = EN/UVLO rising threshold voltage (1.25V)

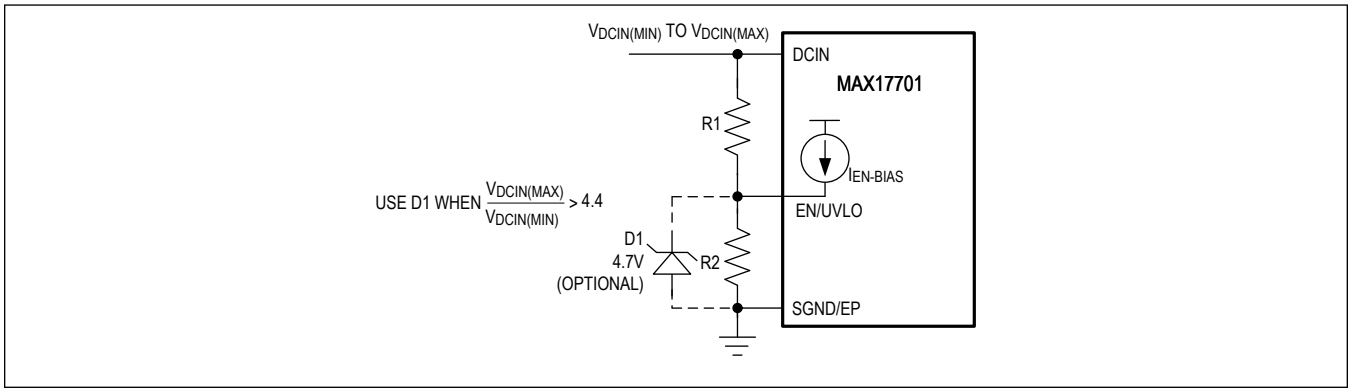


Figure 5. Setting Input-Undervoltage Lockout

Current Regulation Loop Compensation (COMP)

The MAX17701 features a COMP pin to tune the current loop control performance of the average current mode controller. Refer to Figure 1 for a depiction of the compensation network on the COMP pin using R_Z, C_Z, and C_P. The choice of the compensation component values depends on the chosen inductor (L) and its DC resistance (R_{DCR}), switching frequency (f_{SW}), current-sense resistor (R_S), maximum operating input voltage ($V_{DCIN(MAX)}$), the desired regulation voltage across supercapacitor (V_{OUT}), the ESR of the supercapacitor (ESR_{SUP}), and the on-resistances of the step-down converter nMOSFETs ($R_{DS\_ON(HS)}$ and $R_{DS\_ON(LS)}$).

Calculate the compensation resistor R_Z using the following equation:

$$R_Z = \frac{3000 \times L \times f_{SW}}{V_{DCIN(MAX)} \times R_S}$$

Calculate the compensation capacitor C_Z using the following equation:

$$C_Z = \frac{0.8 \times L}{R_Z \times R_E}$$

where

$$R_E = \left[R_{DCR} + R_S + R_{DS\_ON(HS)} \times D_{MIN} + R_{DS\_ON(LS)} \times (1 - D_{MIN}) + ESR_{SUP}\right]$$

$$D_{MIN} = \frac{V_{OUT}}{V_{DCIN(MAX)}}$$

Calculate the high frequency pole capacitor C_P using the following equation:

$$C_P = \frac{0.35}{R_Z \times f_{SW}}$$

Setting the Output Voltage and Voltage Regulation Loop (FB)

The MAX17701 features a FB pin to regulate the voltage across the supercapacitor to a desired level. Connect a feedback resistor divider (R_{TOP} and R_{BOT}) with a compensating capacitor (C_{FB}), as depicted in Figure 1. The choice of feedback components depends on the desired regulation voltage across the supercapacitor (V_{OUT}), the chosen switching frequency (f_{SW}), and the operating input-voltage range ($V_{DCIN(MAX)}$ and $V_{DCIN(MIN)}$).

Calculate R_{TOP} and R_{BOT} using the following equations:

$$R_{TOP} = 10 \times V_{OUT} \ k\Omega$$

$$R_{BOT}=\frac{R_{TOP}}{\left(\frac{V_{OUT}}{V_{FB\_REG}}-1\right)}\ k\Omega$$

where V_{FB_REG} is the FB reference voltage.

Calculate C_{FB} using the following equation:

$$C_{FB}=\frac{0.005}{R_{PAR}\times f_{SW}}\times\frac{V_{DCIN(MAX)}}{V_{DCIN(MIN)}}$$

where

$$R_{PAR}=\frac{R_{TOP}\times R_{BOT}}{R_{TOP}+R_{BOT}}\ \text{in k}\Omega.$$

Output Overvoltage Protection (OVI)

The MAX17701 provides an overvoltage detection comparator at the OVI pin. The overvoltage level for the supercapacitor can be set by connecting OVI to the midpoint of a resistor-divider from output to SGND/EP as shown in Figure 6.

Select R1 in the range of 50kΩ to 100kΩ.

Calculate resistor R2 from the following equation:

$$R2=\frac{R1}{\left(\frac{V_{OUT\_OV}}{V_{OVI\_TH}}-1\right)}$$

where

V_{OUT_OV} = Overvoltage level of the supercapacitor

V_{OVI_TH} = Overvoltage comparator threshold (1.26V)

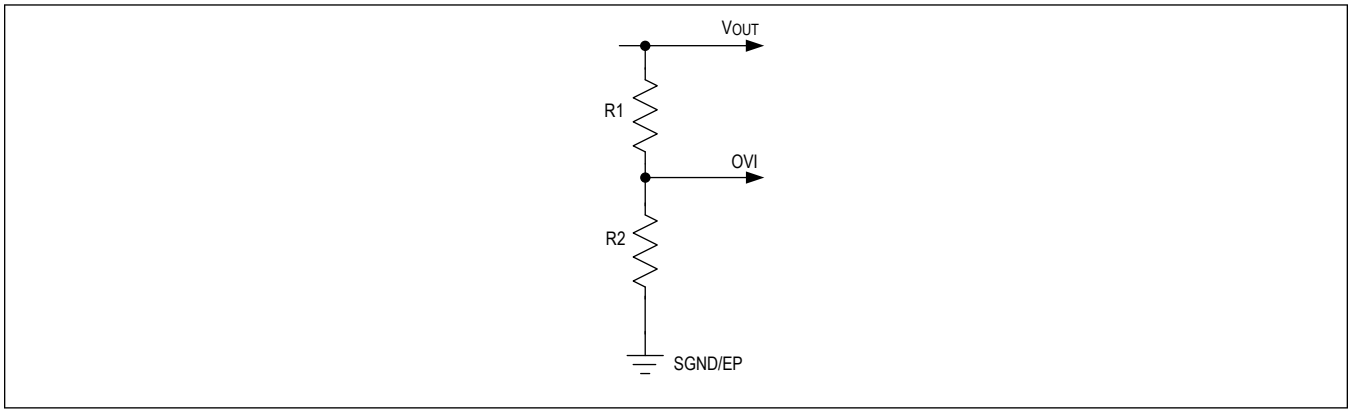


Figure 6. Setting the Supercapacitor Overvoltage Level

Bootstrap Capacitor Selection

Bootstrap capacitance (C_{BST}) value is determined by the selection of the high-side nMOSFET(s). Choose C_{BST} using the following equation:

$$C_{BST}\geq\frac{\Delta Q_G}{\Delta V_{BST}}$$

where:

ΔQ_G = Total gate charge of the high-side nMOSFET(s)

ΔV_{BST} = Voltage variation allowed on the high-side nMOSFET(s) driver after turn-on

Choose $\Delta V_{BST} \leq 100mV$ to select C_{BST}. The bootstrap capacitor should be a low-ESR ceramic capacitor. A minimum value of 0.1µF is recommended.

Input Short-Circuit Protection External nMOSFET Selection

The MAX17701 is designed to control an external logic level nMOSFET that turns Off in less than 100ns and isolates the V_{IN} node from input short-circuit events. This feature prevents discharge of the supercapacitor into the input during input (DCIN) short-circuit events. The external nMOSFET used for this feature only turns On once during power-up and turns Off during shutdown; therefore, the nMOSFET does not need to be optimized for switching performance. This external nMOSFET should therefore be selected with low RDS-On for low forward path conduction losses. The MAX17701 supports external nMOSFETs with gate charge up to 250nC at V_{GS} = 3.9V. Using larger values results in a gate charging time larger than 15ms (t_{GATEN_OK}) and causes the MAX17701 to enter a latched Fault condition.

Step-Down Converter nMOSFET Selection

The MAX17701 drives two external logic-level nMOSFETs to implement the step-down converter high-side and low-side switches. These nMOSFETs must be logic-level compatible with guaranteed on-resistance specifications provided at V_{GS} = 4.5V. The key selection parameters to choose these MOSFETs include:

- On-resistance (R_{DS-ON})
- Maximum drain-to-source voltage ($V_{DS(MAX)}$)
- Miller Plateau voltage on the nMOSFET Gate (V_{MIL})
- Total gate charge (Q_G)
- Output capacitance (C_{OSS})
- Power-dissipation rating and package thermal resistance
- Maximum operating junction temperature

For the step-down converter, nMOSFETs should be chosen in such a way that the switching losses and conduction losses are balanced and optimized. The duty cycles for the high-side and low-side external nMOSFETs can be calculated as follows:

$$D = \frac{V_{OUT}}{V_{IN}}$$

High-side nMOSFET duty cycle: D

Low-side nMOSFET duty cycle: 1 - D

High-side nMOSFET losses can be estimated using the following formula:

$P_{HS-MOSFET} = P_{HS-MOSFET\_Conduction} + P_{HS-MOSFET\_Switching}$

$$P_{HS-MOSFET\_CONDUCTION} = I_{CHG}^2 \times R_{DS-ON(HS)} \times D$$

$$P_{HS-MOSFET\_SWITCHING} = f_{SW} \times \left[\left[\frac{V_{IN} \times I_{CHG}}{2} \times \frac{Q_{SW} \times R_{DR}}{V_{CC} - V_{MIL}}\right] + \left[V_{IN} \times Q_{rr}\right] + \left[\frac{1}{2} \times C_{OSSHS} \times V_{IN}^2\right] + \left[\frac{1}{2} \times C_{OSSLS} \times V_{IN}^2\right]\right]$$

where:
f_{SW} = Switching frequency
I_{CHG} = Charging current
Q_{SW} = Switching charge of the high-side nMOSFET from the nMOSFET data sheet,
R_{DR} = Sum of the DH pin driver pullup resistance and the high-side nMOSFET internal gate resistance,
V_{MIL} = V_{GS} of the high-side nMOSFET that corresponds to $I_D = I_{CHGMAX}$ on the V_{GS} vs. I_D curve in the nMOSFET data sheet

Q_{rr} = Reverse-recovery charge of low-side nMOSFET(s) body diode

C_{OSSHS} = Effective output capacitance of the high-side nMOSFET(s)

C_{OSSLS} = Effective output capacitance of the low-side nMOSFET(s)

Low-side nMOSFET losses can be estimated using the following formula:

$$P_{LS-MOSFET} = I_{CHG}^2 \times R_{DS-ON(LS)} \times (1 - D) + V_D \times I_{CHG} \times t_{DT} \times f_{SW} \times 2$$

where:

V_D = Forward-drop of the low-side nMOSFET(s) body diode

t_{DT} = Dead time (30ns)

Take R_{DS-ON} variation with respect to temperature into account while calculating the power losses and ensure that the losses of each nMOSFET do not exceed their power rating and operate within a safe junction temperature rating. When parallel nMOSFETs are used, it is recommended to use appropriate independent series gate resistors for each nMOSFET to account for gate charge variation from one nMOSFET to another.

Device Power Dissipation

The MAX17701 must dissipate losses due to quiescent current consumption and the internal gate driver.

If V_{CC} is powered from V_{IN}, use the following equation to calculate the approximate IC losses:

$$P_{MAX17701} = V_{IN} \times \left[\left[Q_G \times f_{SW}\right] + I_{QNS}\right]$$

When V_{OUT} is used to power V_{CC} by connecting the EXTVCC pin to an output voltage greater than 4.8V, use the following equation to calculate the approximate IC losses:

$$P_{MAX17701}=V_{EXTVCC} \times \left[\left[Q_G \times f_{SW}\right] + I_{QNS}\right]$$

where:

Q_G = Total gate charge of high-side and low-side nMOSFETs,

I_{QNS} = Input Quiescent current (2.1mA)

Calculate the junction temperature using the following equation and ensure that it does not exceed +125°C.

$$T_J = T_{A(MAX)} + \left(\theta_{JA} \times P_{MAX17701}\right)$$

where:

T_J = Junction temperature

$P_{MAX17701}$ = Power loss in the device

θ_{JA} = Junction-to-ambient thermal resistance

$T_{A(MAX)}$ = Maximum ambient temperature

PCB Layout Guidelines

Careful PCB layout is critical to achieve low losses and low EMI emissions. Use the following guidelines for PCB layout:

- Place ceramic input filter capacitors as close as possible across the drain of the high-side nMOSFET and source of the low-side nMOSFET.
- Route the V_{IN} and DCIN traces from input short-circuit protection nMOSFET source and drain terminals as a differential pair and connect to V_{IN} and DCIN pins of the device. Place V_{IN} and DCIN bypass capacitors close to V_{IN} and DCIN pins, respectively.
- Place V_{CC} and EXTVCC bypass capacitors and the BST capacitor near the respective pins.
- Route switching traces (BST, LX, DH, and DL) away from sensitive signal traces (RT/SYNC, COMP, CSP, CSN and FB).
- The gate current traces must be short in length. Use multiple vias to route these signals if routed from one layer of the PCB to another layer.
- Route current-sense traces as a differential pair to minimize the loop inductance.

- Place a current-sense filter resistor and capacitor near the CSP and CSN pins.
- Place feedback and compensation components close to the device and connect to the SGND/EP copper area.
- Place all power components on the top side of the board and run the power-stage currents using traces or copper fills on the top side only without adding vias wherever possible.
- Keep the power traces and load connections short. Use multilayer, thick copper PCBs (2oz or higher) to enhance efficiency and minimize trace inductance and resistance.
- Allocate a large PGND copper area for the output node and connect the return terminals of the input filter capacitors, output capacitors, and the source terminals of the low-side nMOSFET(s) to that area.
- Refer to the MAX17701 EV kit data sheet for recommended PCB layout and routing.

Typical Application Circuit

20A Supercapacitor Charger

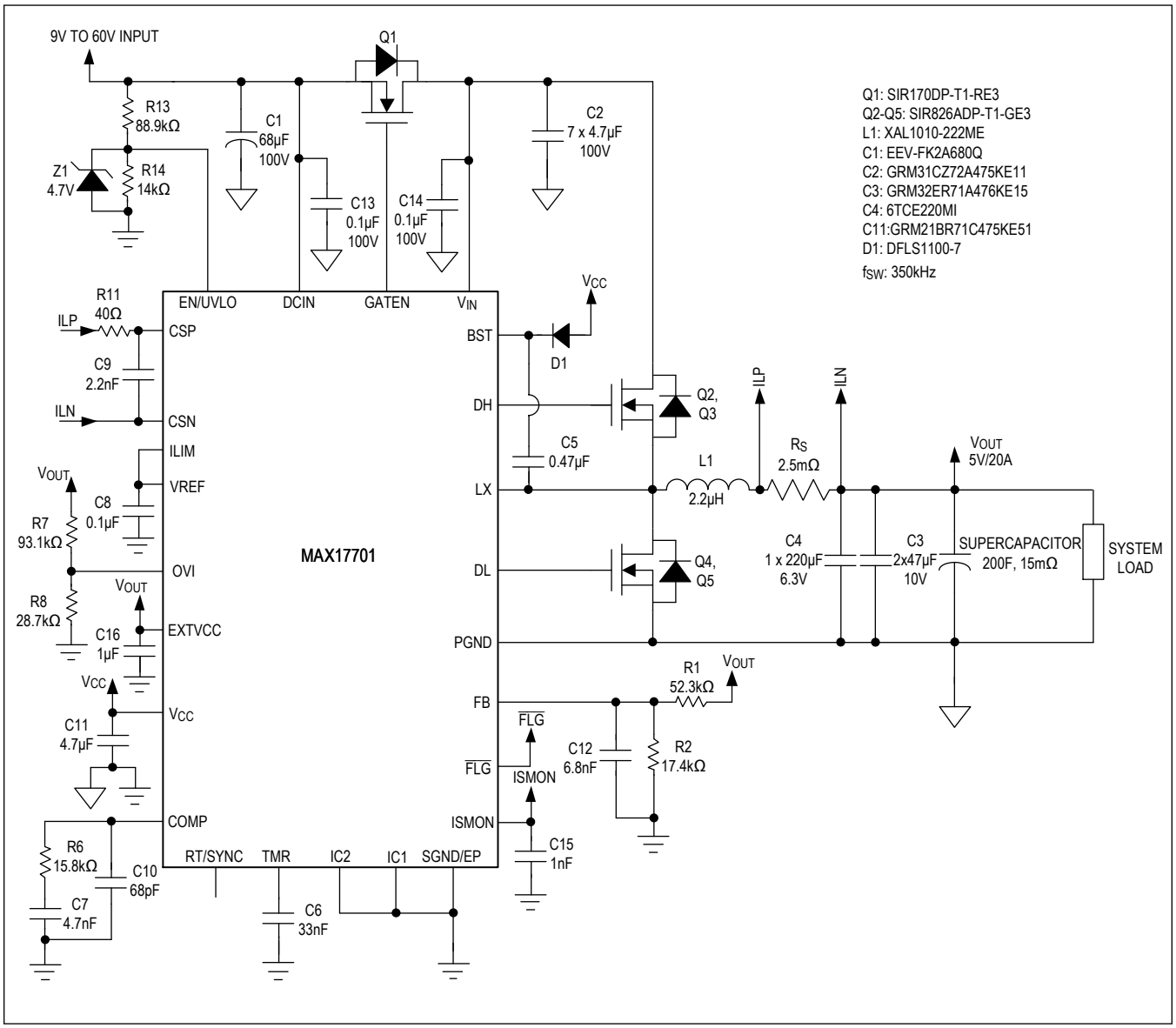


Figure 7. 5V/20A Supercapacitor Charger

Typical Application Circuit (continued)

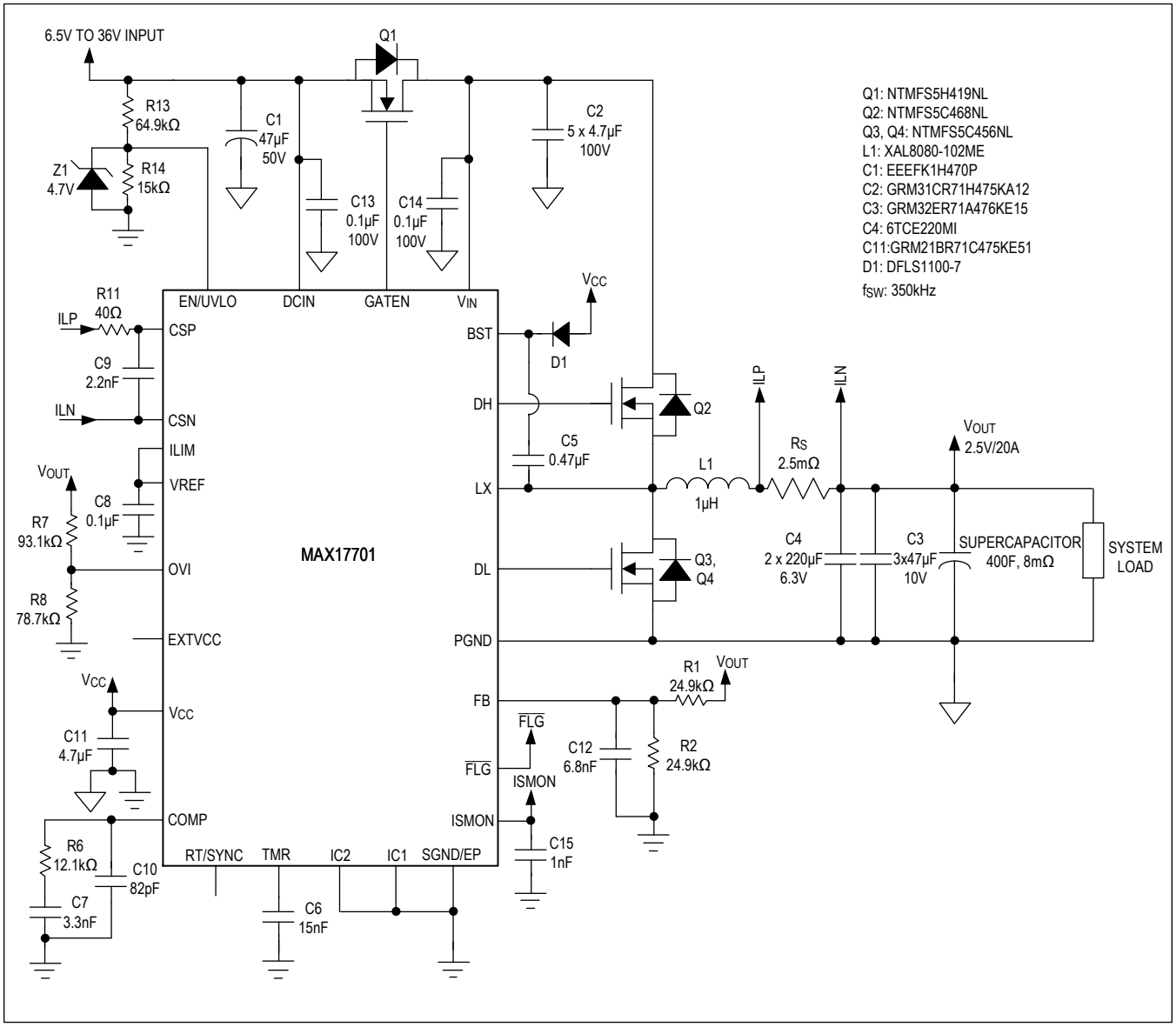


Figure 8. 2.5V/20A Supercapacitor Charger

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE
MAX17701ATG+	-40ºC to +125ºC	24 TQFN-EP
MAX17701ATG+T	-40ºC to +125ºC	24 TQFN-EP

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/20	Initial release	—
1	6/20	Updated the *General Description, Benefit and Features, Simplified Application Circuit, Absolute Maximum Ratings, Electrical Characteristics, Detailed Description, Operating Input-Voltage Range, CC Mode Charging Current Settings (ILIM), Step-Down Converter nMOSFET Selection,* and *Typical Application Circuit* (Figures 7 and 8) sections	1–2, 6, 13, 21–23, 27, 29–30